

Robust, low-cost, auditable random number generation for embedded system security

Ben Lampert^{*○}, Riad S. Wahby^{*},
Shane Leonard^{*}, and Philip Levis^{*}

^{*}Stanford University
[○]NAUTO, Inc.

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All secure systems depend on random numbers

10 DO YOU KNOW 
AM WHERE YOUR
RANDOM NUMBERS
COME FROM?



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Embedded systems face unique challenges

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We present a hardware/software system for random number generation tailored to embedded devices:

- hardware costs \approx \$1.50, 1.5 cm² board area
- run once at boot, takes 25 ms to initialize
- energy cost equivalent to 10 ZigBee packets

Debian Bug Leaves Private SSL/SSH Keys Guessable



670



Posted by timothy on Tuesday May 13, 2008 @11:01AM from the security-is-a-process dept.

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```
int getRandomNumber()  
{  
    return 4; // chosen by fair dice roll.  
             // guaranteed to be random.  
}
```

<http://xkcd.com/221/> CC BY-NC 2.5

A deterministic “random” number generator?

What properties would it have?

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Idea: add a secret!

Cryptographically secure pseudorandom number generator

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Figure of merit: *entropy*

informally: the number of bits in k that an adversary does not know

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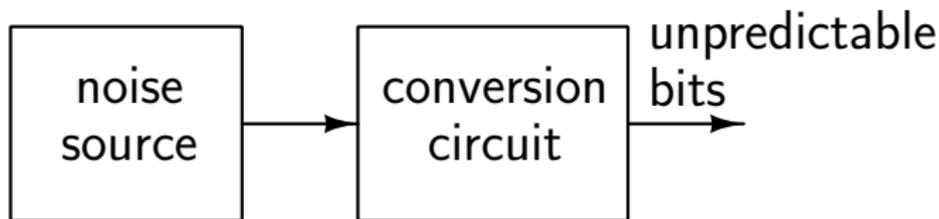
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 - ✗ Embedded processors may not have RNG
 - ✗ Integrated RNG is opaque, not auditable
 - Becker et al. [CHES '13] showed that integrated hardware RNGs can be stealthily backdoored

Wish list

- Inexpensive
- Small
- Low power
- Insensitive to environmental factors (e.g., temperature, RF interference)
- Easy to detect failure: simple and auditable
- Generates a CSPRNG key quickly

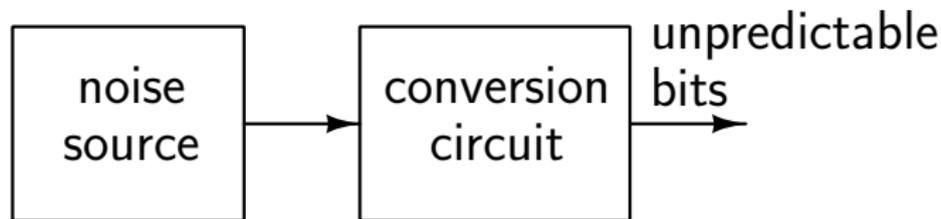
Generating unpredictable bits: two easy pieces



Noise source: a device exhibiting
an unpredictable physical phenomenon

Conversion circuit: detects state of device,
produces corresponding bits

Generating unpredictable bits: two easy pieces



Example noise sources:

Radioactive decay

Beam splitting

Photoelectric effect

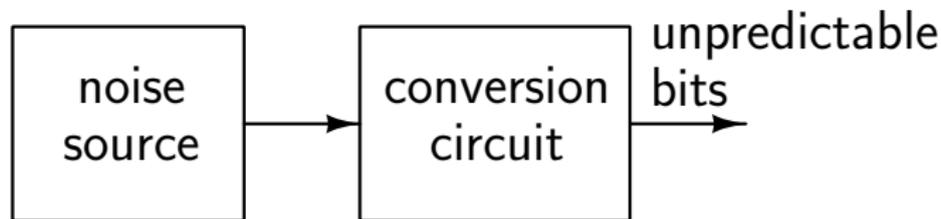
Circuit noise

thermal noise (all electronic devices)

shot noise, flicker noise (diodes and transistors)

Zener noise, avalanche noise (diodes)

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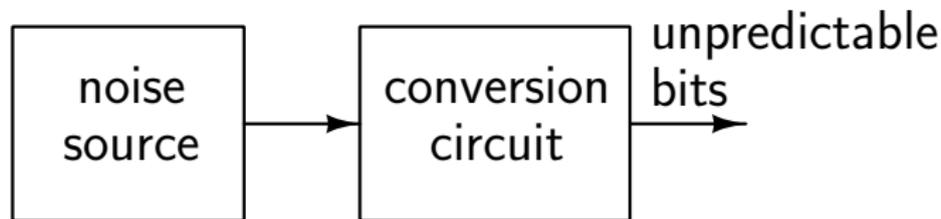
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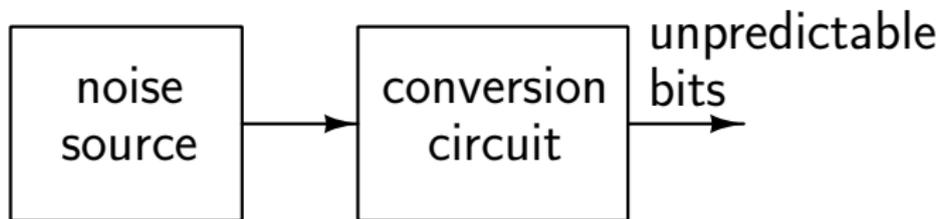
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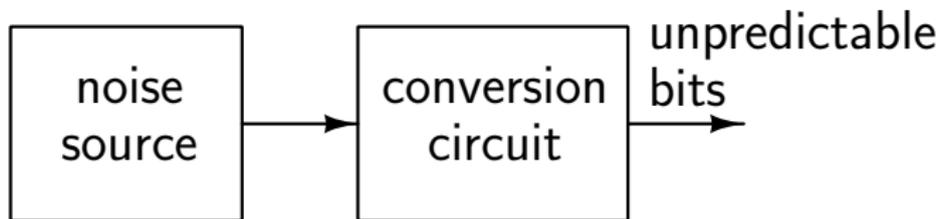
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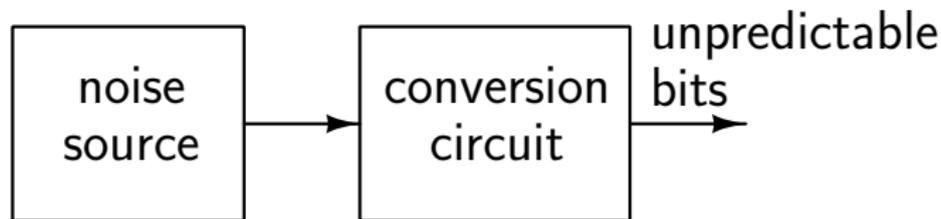
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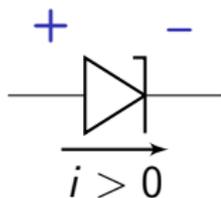


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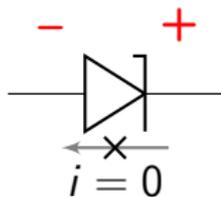
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Diodes, reverse breakdown, and avalanche

Voltage applied in forward direction:
current can flow

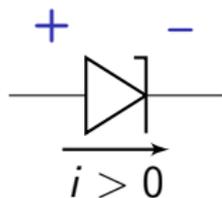


Low voltage applied in reverse
direction: current cannot flow

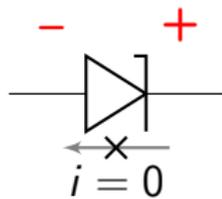


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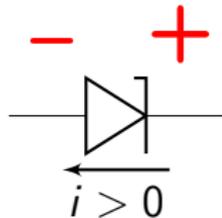
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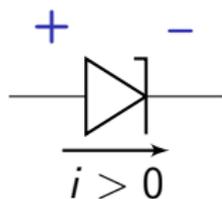


High voltage applied in reverse
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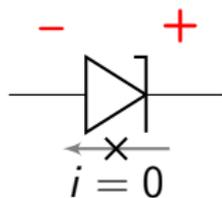


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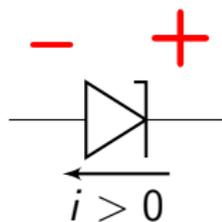
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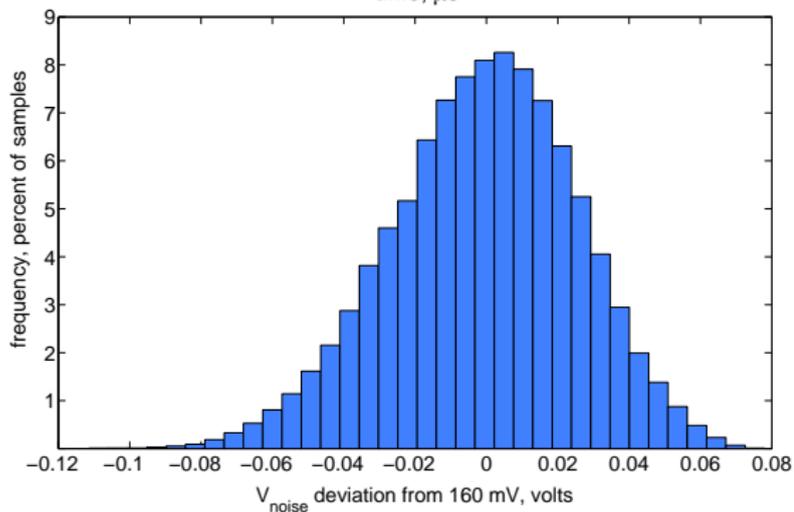
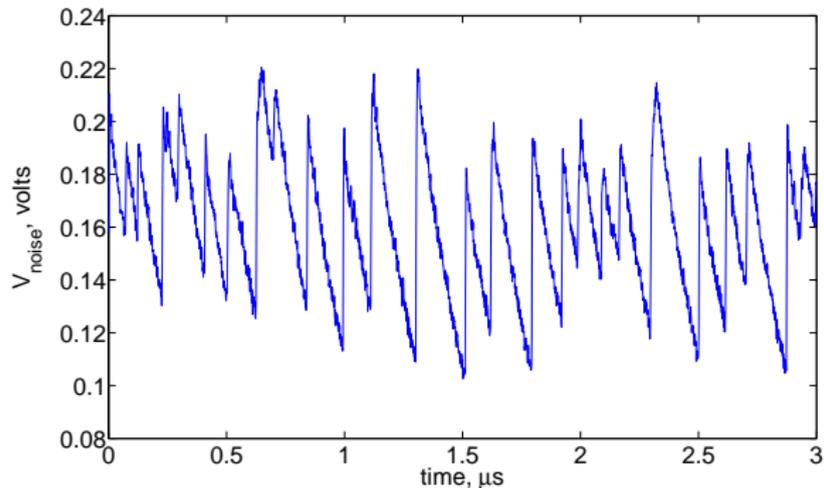
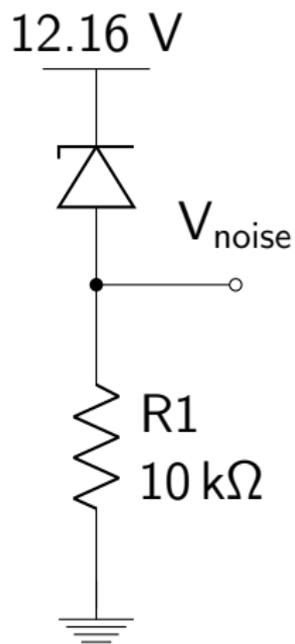
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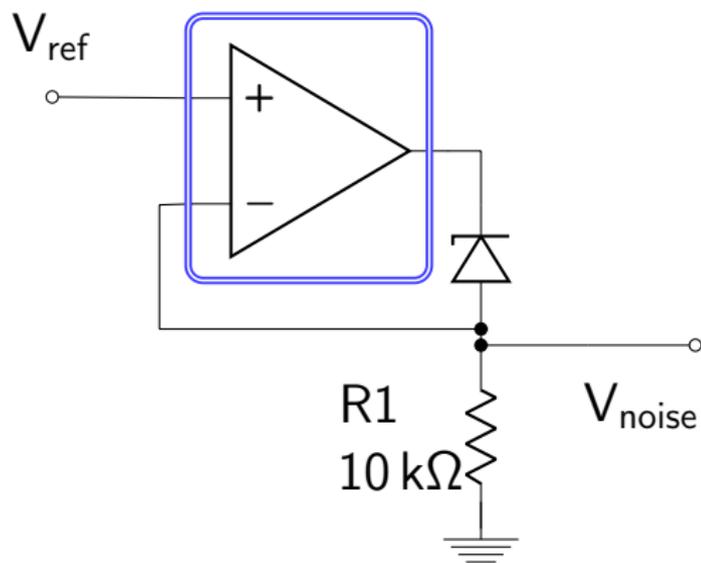
Avalanche current:

electron collisions cause an “avalanche” of charge carriers

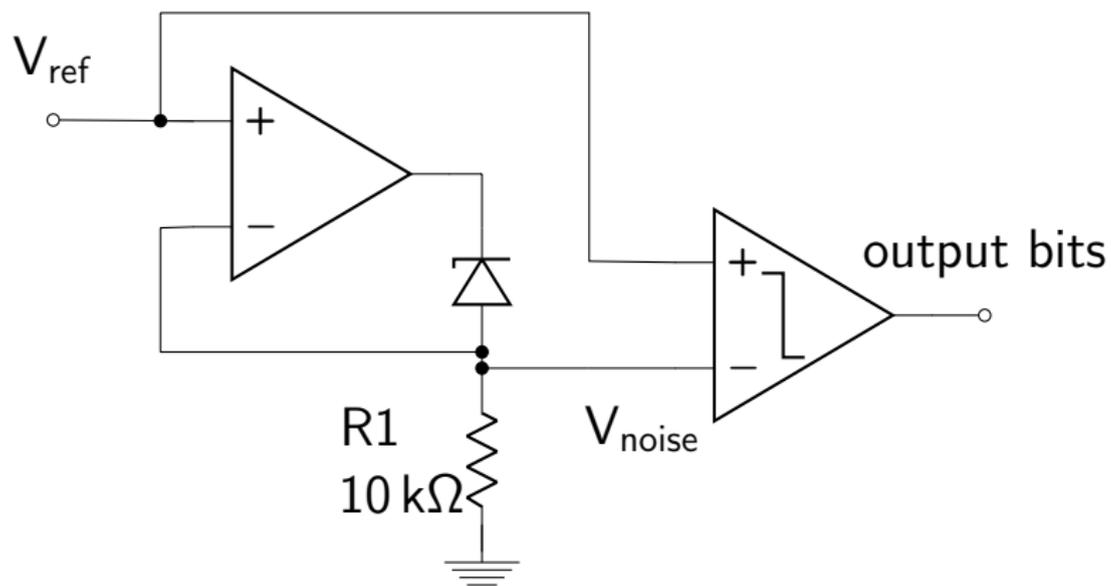
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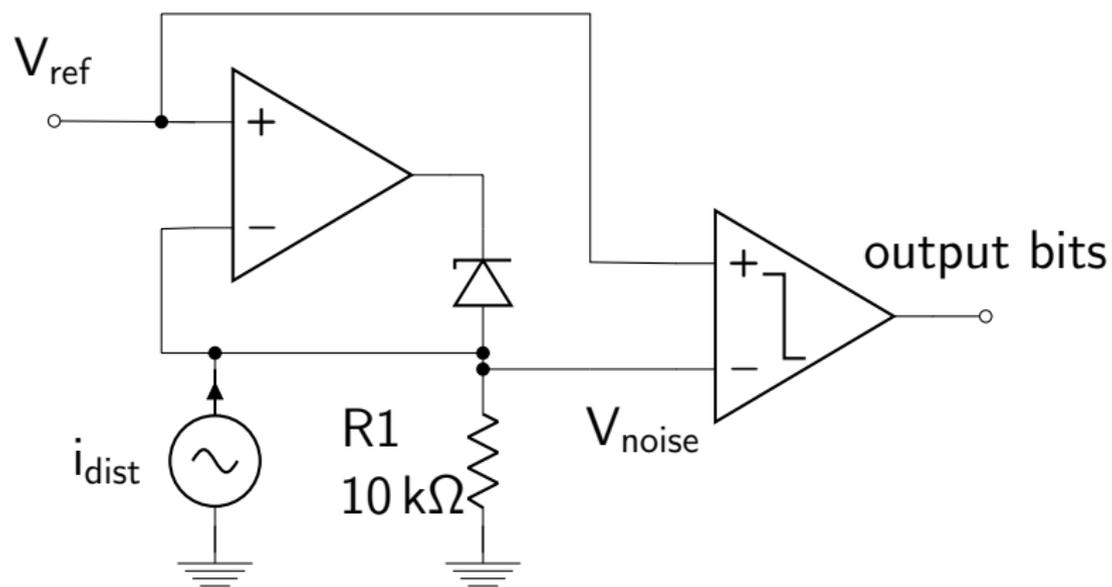
Overcoming manufacturing variations



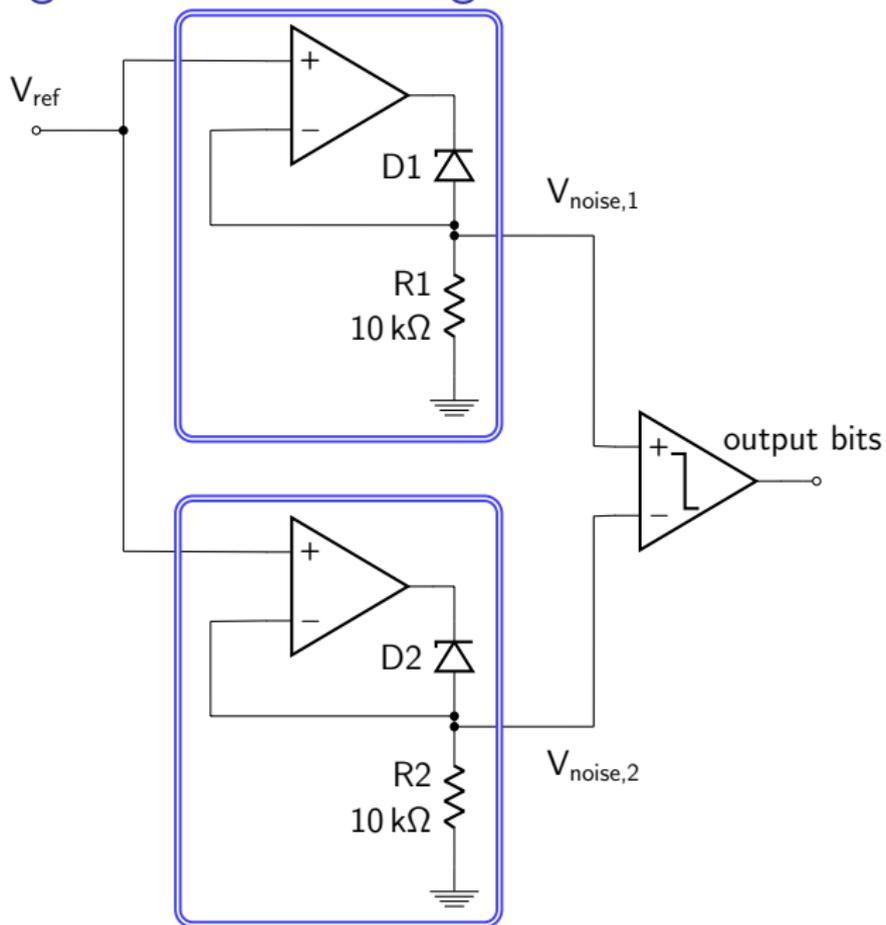
Converting V_{noise} to bits



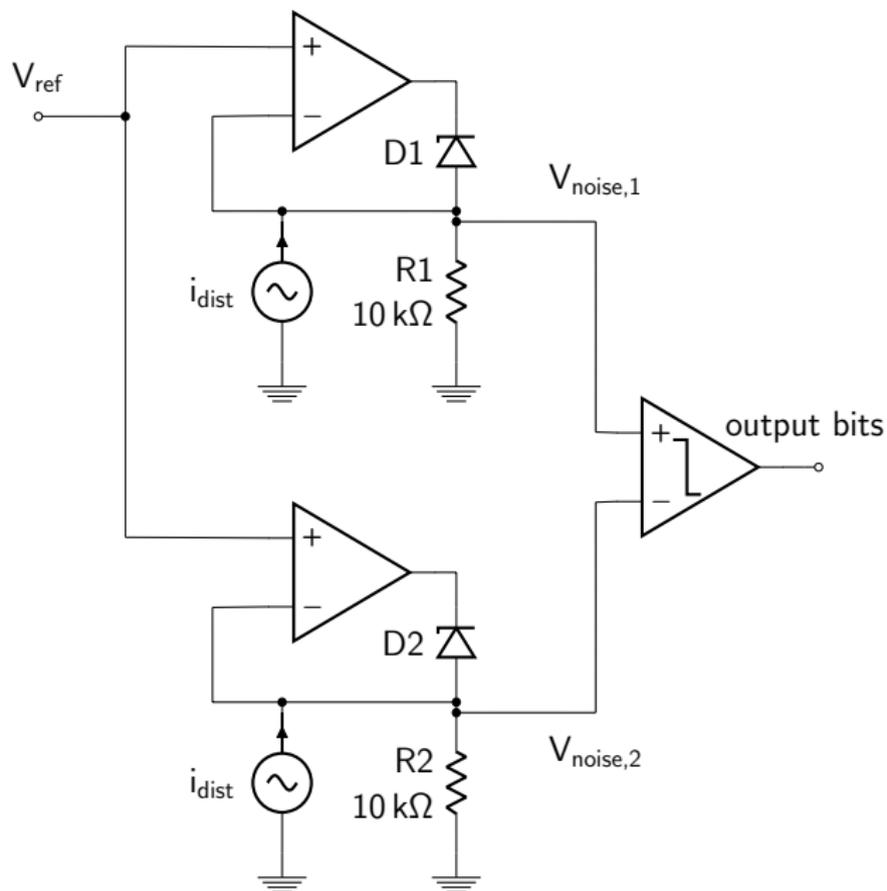
Issue: outside disturbances



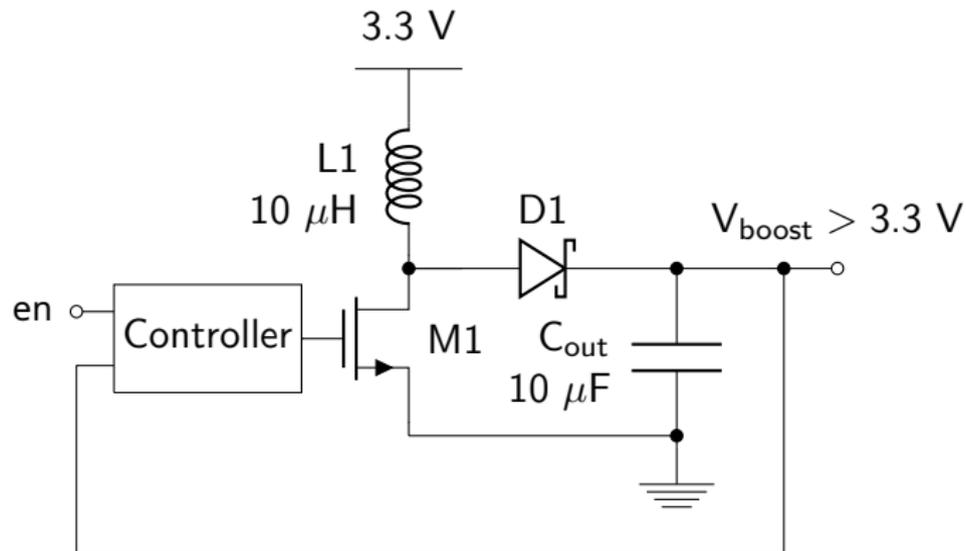
Overcoming disturbances using a differential circuit



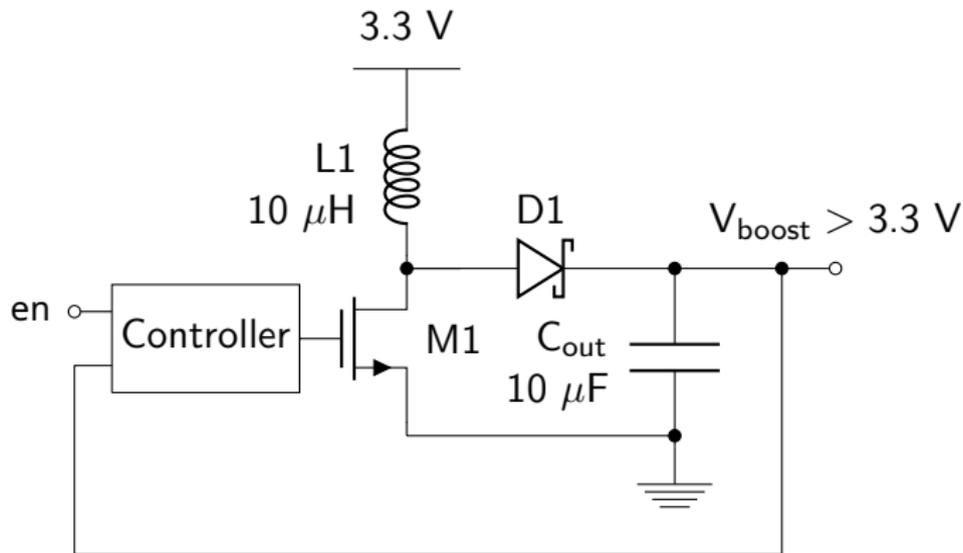
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Issue: how do we generate 12 V?

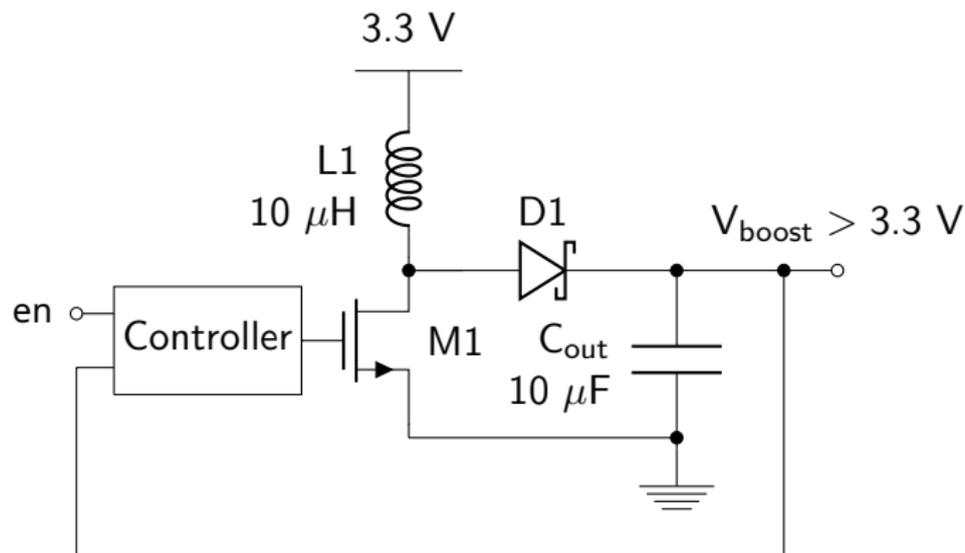


Issue: how do we generate 12 V?



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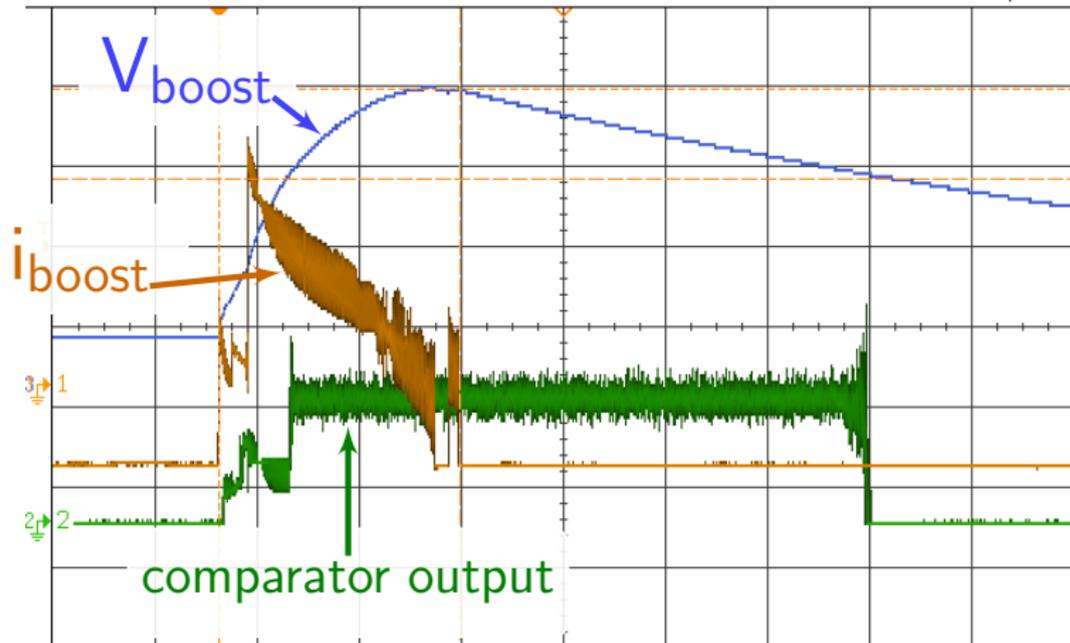
Issue: the boost converter causes **large disturbances**

Solution: interleave boost and output sampling

Interleaved boost operation

MSO-X 3054A, MY53480236: Fri Apr 08 07:02:34 2016

1 50% / 2 1.00V / 3 5.00V / 4 16.90ms 5.000ms / Stop f 1 86.3%



Agilent

Acquisition
High Res
10.0MSa/s

Channels

DC	10.0:1
DC	10.0:1
DC	10.0:1
DC	1.00:1

Cursors

ΔX :
+11.800000000ms

$1/\Delta X$:
+84.746Hz

$\Delta Y(3)$:
-5.5625V

Cursors Menu

Mode Manual Source 3 Cursors X2 Units X1: 0.0s Y1: 18.4375V X2: 11.800000000ms Y2: 12.8750V

Putting it all together

- At boot:
 1. run circuit to gather 1024 bits, b_{raw}
 2. compute $k = \text{SHA256}(b_{\text{raw}})$
 3. initialize global counter $c = 0$

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 1. run circuit to gather 1024 bits, b_{raw}
 2. compute $k = \text{SHA256}(b_{\text{raw}})$
 3. initialize global counter $c = 0$
- To generate a random number:
 1. increment counter c
 2. use AES to encrypt c under key k
 3. return resulting ciphertext

Testing and monitoring

In the paper, we define methods for:

Acceptance testing:

after assembly and before deployment, each device should be checked for proper operation

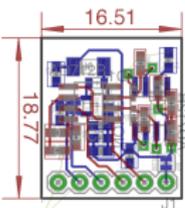
Online auditing:

for systems requiring high assurance, further online testing in the field

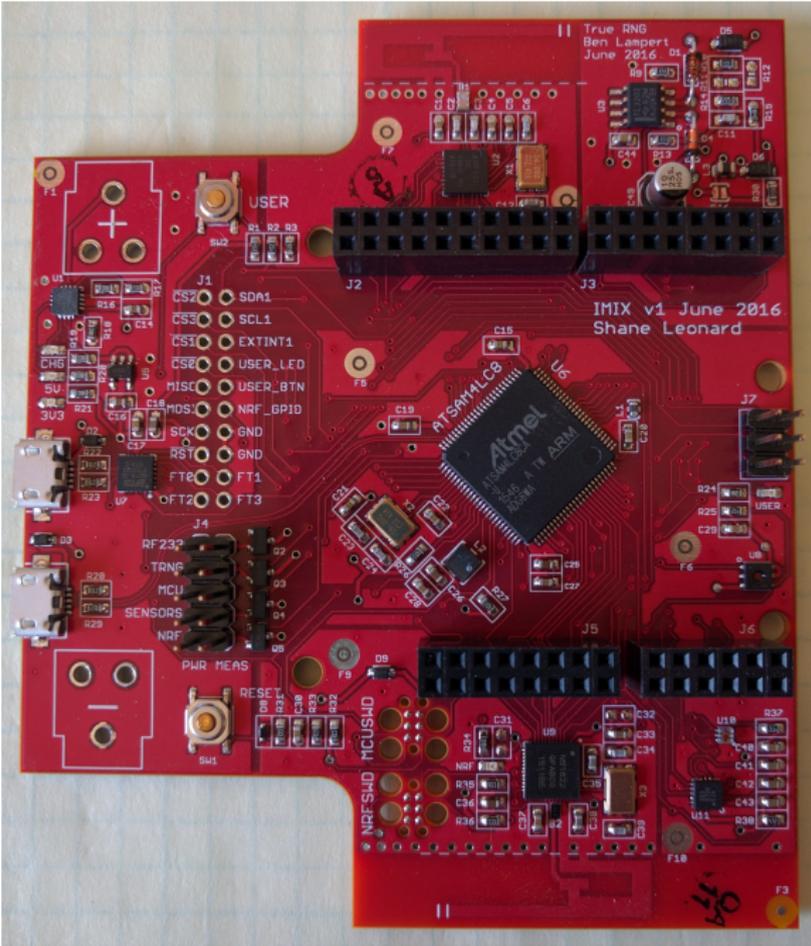
Evaluation questions

- How quickly should the system sample the bit generator's output?
- What are the statistical properties of the raw output versus time and temperature?
- What is the cost, in energy and time, of generating a CSPRNG key?

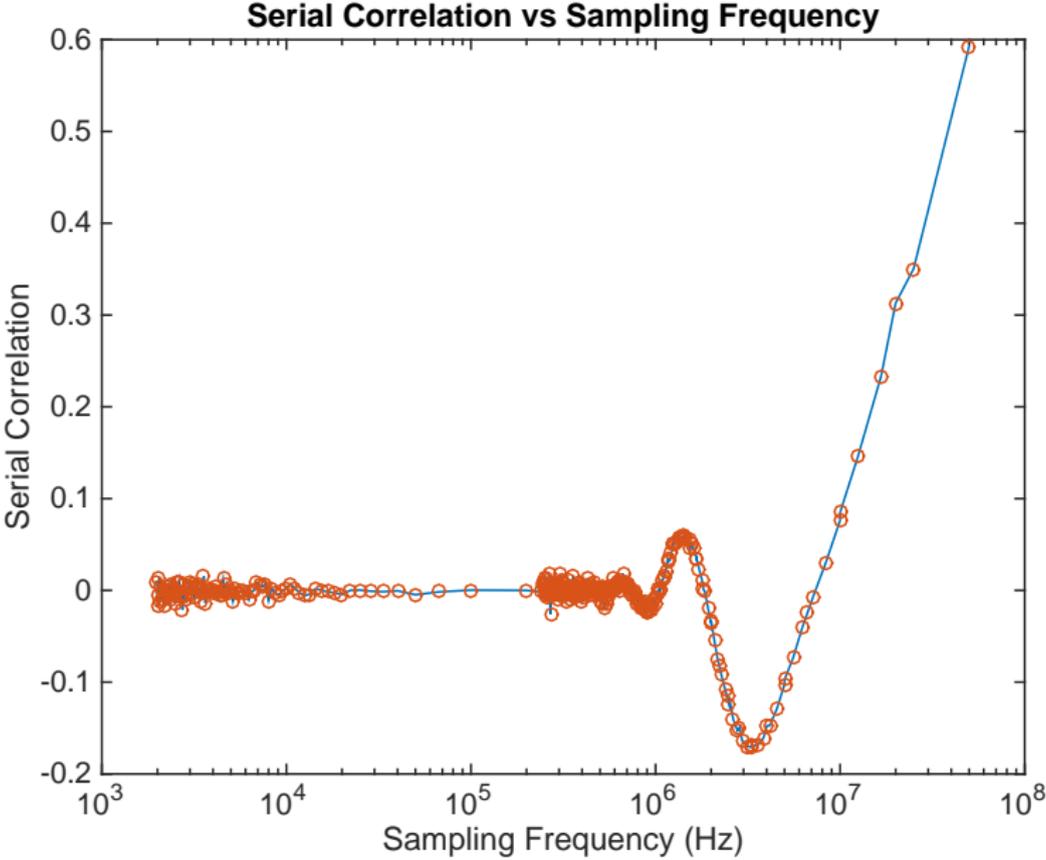
Built systems



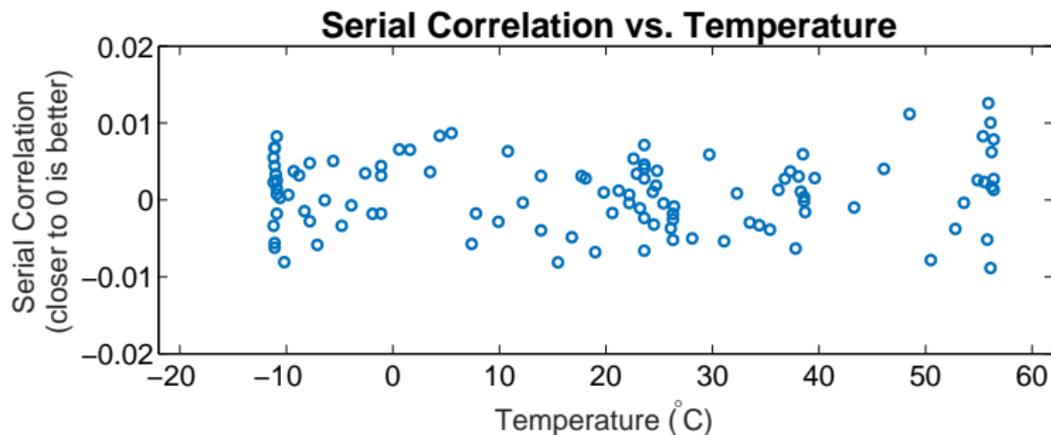
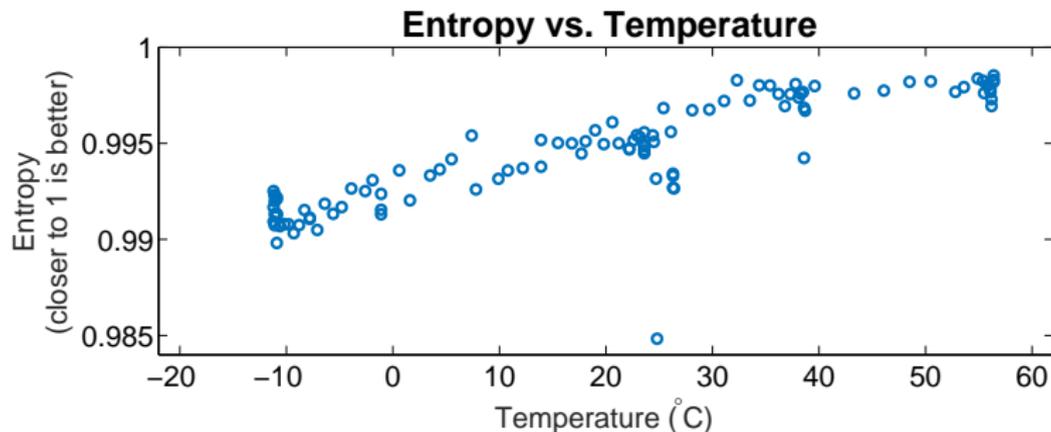
Cost \approx \$1.50



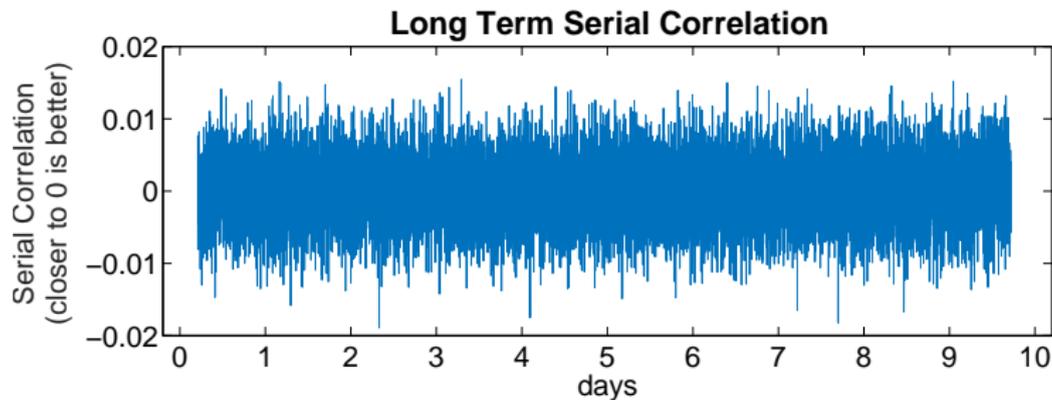
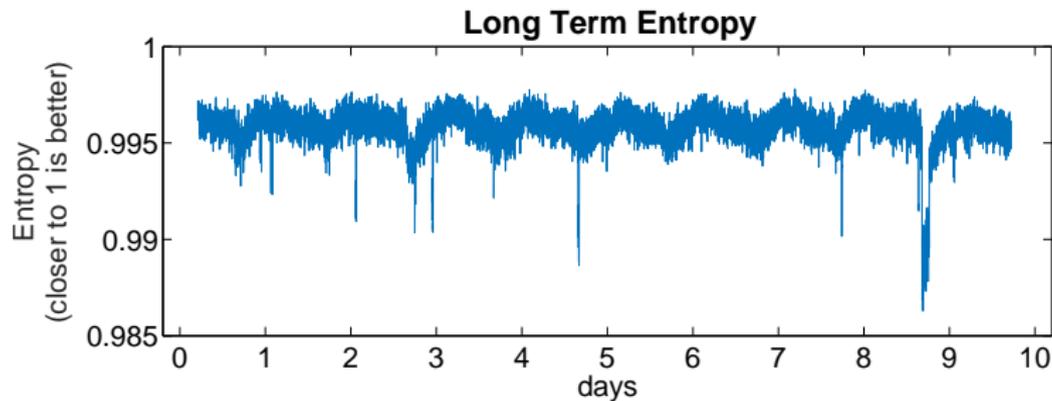
Determining the sample rate



Statistical properties versus temperature



Statistical properties versus time



Time and energy costs to generate CSPRNG key

Time to gather 1024 bits:

≈13 ms running dc/dc converter

≈12 ms sampling output of bit generator

Energy to gather 1024 bits:

≈3 μ J per bit

≈ 10× more energy per bit than a ZigBee radio,
amortized over all CSPRNG outputs

Conclusions

- You should worry about your random numbers!
- A CSPRNG can generate secure, effectively limitless output given a hard-to-guess key. . .
- . . .but in embedded systems, generating a CSPRNG key is challenging
- We have presented a design tailored to embedded systems for secure, inexpensive pseudorandomness
- Future work: smaller, cheaper, faster

<https://github.com/helena-project/imix>

